

Requested Patent: JP1028856  
Title: MULTILAYERED INTEGRATED CIRCUIT  
Abstracted Patent: JP1028856  
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Equivalents:

**ABSTRACT:**

**PURPOSE:** To form a large scale integrated circuit with high reliability, by stacking, on an LSI chip of lower side layer, an LSI chip whose area is smaller than that of the LSI chip of lower side layer, and connecting, through wires, the LSI chip of the upper side layer and that of the lower side layer.

**CONSTITUTION:** A multilayer integrated circuit is formed, by stacking at least two or more layers of large scale integrated circuit chips 10-12. The area of the chip 11 of upper layer stacked on the chip 10 of lower layer is larger than the area of the chip 12 of upper layer stacked on the chip 11 of lower layer. The signal transmission and reception between the chip 10 and the chip 11 and between the chip 11 and the chip 12 is performed via a wire 15a. Thereby, a large scale integrated circuit with high reliability can be obtained.